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| 09/552,085 | 02/24/2000 | Tsutomu Ishikawa | | 6265 |

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CANTOR COLBURN, LLP
55 GRIFFIN ROAD SOUTH
BLOOMFIELD, CT 06002

| EXAMINER |
|---|
| NGUYEN, LONG T |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 09/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/552,085 | Applicant(s) ISHIKAWA ET AL. | |
|---|---|---|---|
| | Examiner Long Nguyen | Art Unit 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *11-14,16-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-14,16-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Amendment*

1. The amendment filed on 6/26/03 has been received and entered in the case.

2. In this office action, the allowability of claims 11-14, 16-18 and 20 in the last office action are withdrawn based on the rejection as discussed below.

### *Claim Objections*

3. Claim 18 is objected to because of the following informalities: "a source" on line 2 of claim 18 should be changed to --the source--. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 17, the phrase "said source follower circuit comprises a field effect transistor integrated on said semiconductor substrate, said field effect transistor having a gate connected to said pad" is indefinite because it is not known whether the field effect transistor recited in the above phrase is the same as the transistor (claim 11, line 3) recited earlier or a different transistor. To overcome this problem, it is suggest that "said source follower circuit comprises a field effect transistor" on line 2 of claim 17 be changed to --said transistor of said source follower circuit is a field effect transistor--; and "substrate, said field effect transistor having a gate connected to said pad." on line 3 of claim 17 be changed to --substrate.-- because

"a gate connected to said pad" on line 3 of claim 17 has already been recited earlier (line 3 of claim 11).

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 11-14 and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Bowers (USP 4,675,561).

With respect to claim 11, Figures 6-7 of the Bowers reference disclose a circuit a semiconductor integrated circuit which includes: a pad (88, Figure 7) to which an input signal (Vin) is externally inputted; a source follower circuit (FET2 and I2 in Figure 6) including a transistor (FET2) having a gate connected to the pad (88, Figure 7) and a source (84, Figure 7) for producing an output signal (72, Figure 6); and it is inherent that a parasitic capacitance (of FET1 and FET2) is created between said pad and a semiconductor substrate 76 (e.g. the parasitic capacitance between the gate and the body of FET1 and FET2), and said source of the source follower circuit (e.g. source of FET2) is connected to the semiconductor substrate side of the parasitic capacitance (see Figure 7) so as to charge and discharge the parasitic capacitance by the output signal of the source follower circuit; an island region (90, Figure 7) on the upper surface of the semiconductor substrate (76) containing impurities of a second conductivity type (P), and the pad formed on the island region via an oxide film (the oxide film right underneath of pad 88); and wherein the semiconductor substrate (76) contains impurities of a first conductivity type (N);

and wherein an output terminal of the source follower circuit is connected to the island region (the wire connected the source 84 in Figure 7 to the island region 90 in Figure 7). Note that although the output (72) of the source follower circuit in Figure 6 is connected to the source (84, Figure 7) and the body (90, Figure 7), given "island region" its broadest reasonable interpretation, it is reasonable to consider the body region (90, Figure 7) as an "island region".

With respect to claim 12, it is seen in Figure 7 that the island region (90) is surrounded with an isolation region (78) containing impurities of the first conductivity type (N).

With respect to claim 13, it is seen in the Bowers reference that the first conductivity type is a P-type and the second conductivity type is an N-type (Figure 7 and Col. 5, lines 42-48).

With respect to claim 14, it is seen in Figures 6-7 of the Bowers reference that the output terminal (source of FET2) of the source follower circuit is connected to the island region by way of a metal conductor.

With respect to claim 16, it is seen in Figure 6 that the source follower circuit includes an amplifier (FET2).

Insofar as understood in claim 17, it is seen in Figure 6 that the transistor (FET2) of the source follower circuit is a FET transistor (FET2) integrated on the semiconductor substrate.

With respect to claim 18, it is seen in Figure 6 that the FET transistor (FET2) has a drain connected to a power source, and the source connected to the ground via a constant current source (I2) for providing the output signal.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bowers (USP 4,675,561) in view of Choi et al. (USP 4,700,461).

With respect to claim 20, Figure 6-7 of the Bowers reference discloses a circuit which includes all of the claimed limitations except that each of the transistors of the circuit in Figure 6-7 is junction field effect transistor (JFET). However, the Choi et al. reference teaches that the JFET has inherent advantages over the MOSFET for certain applications such as JFETs being more suitable for high temperature operation than MOSFETs (Col. 1, lines 41-45). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the circuit in Figure 6-7 of the Bowers reference to use junction field effect transistors (JFETS) instead of MOSFETs, e.g., using JFET devices for all the transistors in the circuit in Figure 6-7 of the Bowers reference, for the purpose of high temperature operation of the circuitry. Thus, because Figures 6-7 of the Bowers reference meets all the structure of the claim limitation, so this modification meets all the method claim limitations of claim 20, i.e., the modification circuit would meet the step of controlling a chagrining amount of a parasitic capacitance of a JFET (FET2 in Figure 6-7 of Bowers in the above modification) by changing the input signal (i.e., the input signal varies from H to L and vice versa), wherein controlling the charging amount of the parasitic capacitance (parasitic capacitance of FET2) including

connecting a source follower circuit (FET2 and I2 in Figure 6) to a pad (88 in Figure 7, i.e., gate of FET2) and connecting an output terminal (72, Figure 6) of the source follower circuit to an island region (90, Figure 7) disposed between the pad and a semiconductor substrate (76). Note that the pre-ample "reducing an attenuation of an input signal to a JFET" is also met because the structure of the claim is fully met, and the above modification using JFET to fabricate the circuit.

***Conclusion***

10. If applicant believes that an interview with the examiner would be helpful in prosecution this case, please feel free to call the examiner at (703) 308-6063.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

LN
Date: 8/19/03

Long Nguyen
Art Unit: 2816